[0014] FIG. 2 is a high-level partial schematic diagram illustrating a desirable boundary scan methodology that utilizes only one scan clock tree;

[0015] FIG. 3 is a high-level partial schematic diagram illustrating a known problem with implementing the single scan clock methodology of FIG. 2;

[0016] FIG. 4 is a high-level partial schematic diagram partially illustrating edge-triggered shift register latches (SRLs) of the present invention that may be used with the single scan clock methodology of FIG. 2 to eliminate the problem illustrated in FIG. 3;

ler 5/25/09 [0017] FIGS. 5A ~~and 5B~~ 5C are schematic diagrams of two MUX-type edged-triggered SRLs of the present invention; FIG. C is a schematic diagram of a non-MUX-type edge-triggered SRL of the present invention;

[0018] FIGS. 6A and 6B are plots of the states of various signals within the MUX-type edge-triggered SRL of FIG. 5A during, respectively, test operation and functional operation;

[0019] FIGS. 7A and 7B are plots of the states of various signals within the non-MUX-type edge triggered SRL of FIG. 5C during, respectively, test operation and functional operation; and

[0020] FIGS 8A and 8B are, respectively, a high-level partial